

Application No.: 10/015,414

Docket No.: JCLA7737

### AMENDMENTS TO CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

#### **Claims 1-4 (previously canceled)**

5. (Currently Amended) A method of erasing a non-volatile memory cell with a nitride tunneling layer, the non-volatile memory comprising:

a substrate;

a nitride tunneling layer disposed on the substrate;

a charge-trapping layer comprising electron holes, disposed on the nitride tunneling layer;

a dielectric layer disposed on the charge-trapping layer;

a gate conductive layer disposed on the dielectric layer; and

a source region and a drain region disposed in the substrate beside the gate conductive layer;

the method comprising the steps of:

~~programming the charge-trapping layer with hot electron holes; and~~

applying a first positive bias to the drain region, applying a second positive bias to the gate conductive layer, and grounding the source region and the substrate ~~to generate hot electrons/electron holes in a channel region~~, wherein said hot electrons are injected into the

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charge-trapping layer through the nitride tunneling layer, and wherein said hot electrons combine with hot electron holes in the charge-trapping layer to erase the non-volatile memory cell.

6. (Original) The method of claim 5, wherein the first positive bias ranges from about 2V to about 5V.

7. (Original) The method of claim 5, wherein the second positive bias ranges from about 2.5V to about 5V.

8. (Currently Amended) The method of claim 5, wherein the first positive bias and the second positive bias are both sufficient to erase ~~lower than those adopted for erasing a substrate-oxide-nitride-oxide-silicon (SONOS) memory having a same size as the non-volatile memory with the nitride tunneling layer.~~